**CHAPTER1**

* 1. **INTRODUCTION:**

The aim of this project is to scroll a message on LCD display from a PC or a key board. This scrolling message board is not a simple message box. Instead of showing a static text,It scrolls the text to maximize visitors attention.Generally a situation may come where we need to display message from our keyboard on to LCD directly and it is achieved by making an interface from pc to an LED using “ARM processor”. ARM is abbreviated as ADVANCED RISC MACHINE

* 1. **BlocKDiagram:**

**1.3 CIRCUIT DIAGRAM:-**



* 1. **OPERATION:-**
* Switch on the power supply to the transmitter section after making necessary connections. A 230V/50Hz ac is stepped down to 12V/50Hz ac.tis is voltage is fed to a bridge rectifier an filter circuit.
* The output of filter circuit is fed to IC7812&IC7805 ,the output of 7805 inturn is connected to ARM controller module which works with +5v dc supply.
* The o/p from pc is given to the i/p of the MAX232,the power supply is given to the pin no 16(Vcc) & pin no 15(GND),
* The o/p from the pc is applied to the i/p of the MAX 232 at the pin no 13(RIN)&14(TXOUT).The o/p from the MAX 232 is obtained at the pin no’s 11(T1IN),12(R1OUT),10(T2IN),9(R2OUT).
* The o/p from the MAX232 is given as the i/p to the ARM controller.
* The power supply to ARM controller is given to the Vcc at the pin no’s (7,23,43,51) & GND at the pin no’s(6,25,42,50).The o/p from the MAX 232 has been given to the P0.0 –TXD0(pin no 19),P0.1-RXD0(pin no 21),P0.8-TXD1(pin no 33),P0.9-RXD1(pin no 34).The crystal oscillator is connected to the pin no 3 (RTCXTL1)&pin no 5 (RTCXTL2) to the ARM controller.
* The o/p of the ARM controller is applied to LCD.
* Tthe power supply is given to the pin no 2 to Vcc and 1 to GND,the o/p from the ARM controller is applied to i/p of the lcd pin no’s from 4 to 14 .Pin no 4 is connected to pin no 37 (P0.11-CTS1/CAP1.1/SCL1),pin no 5 is connected to pin no 38(P0.12-DSR1/MAT 1.0/AD 1.3) ,pin no 6 is connected to pin no 39(P0.13-DTR1/MAT 1.1/AD 1.4),pin no 7 is connected to pin 16(P1.16-TRACEPKT0), pin no 8 is connected to pin 12(P1.17-TRACEPKT1), pin no 9 is connected to pin 8 (P1.18-TRACEPKT2), pin no 10 is connected to pin 4(P1.19-TRACEPKT3), pin no 11 is connected to pin 48(P1.20-TRACESYNC), pin no 12 is connected to pin 44(P1.21-PIPESTAT0), pin no 13 is connected to pin 40(P1.22-PIPESTAT1), pin no 14 is connected to pin 36(P1.23-PIPESTAT2).
* Finally the o/p is display on the LCD screen.

**1.5 KEY BOARD**

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**CHAPTER 2**

**POWER SUPPLY**

**2.1 Introduction:**

The input to the circuit is applied from the regulated power supply. The a.c. input i.e., 230V from the mains supply is step down by the transformer to 12V and is fed to a rectifier. The output obtained from the rectifier is a pulsating d.c voltage. So in order to get a pure d.c voltage, the output voltage from the rectifier is fed to a filter to remove any a.c components present even after rectification. Now, this voltage is given to a voltage regulator to obtain a pure constant dc voltage.

**Block Diagram:**

**2.2 Transformer:**

Usually, DC voltages are required to operate various electronic equipment and these voltages are 5V, 9V or 12V. But these voltages cannot be obtained directly. Thus the a.c input available at the mains supply i.e., 230V is to be brought down to the required voltage level. This is done by a transformer. Thus, a step down transformer is employed to decrease the voltage to a required level.

**2.3 Rectifier:**

The output from the transformer is fed to the rectifier. It converts A.C. into pulsating. D.C. The rectifier may be a half wave or a full wave rectifier. In this project, a bridge rectifier is used because of its merits like good stability and full wave rectification.

**2.4 Filter:**

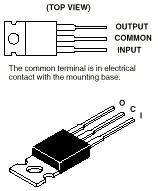
Capacitive filter is used in this project. It removes the ripples from the output of rectifier and smoothens the D.C. Output received from this filter is constant until the mains voltage and load is maintained constant. However, if either of the two is varied, D.C. voltage received at this point changes. Therefore a regulator is applied at the output stage.

**2.5 Voltage Regulator:**

As the name itself implies, it regulates the input applied to it. A voltage regulator is an electrical regulator designed to automatically maintain a constant voltage level. In this project, power supply of 5V and 12V are required. In order to obtain these voltage levels, 7805 and 7812 voltage regulators are to be used. The first number 78 represents positive supply and the numbers 05, 12 represent the required output voltage levels.A variable regulated power supply, also called a variable bench power supply, is one where you can continuously adjust the output voltage to your requirements. Varying the output of the power supply is the recommended way to test a project after having double checked parts placement against circuit drawings and the parts placement guide.

This type of regulation is ideal for having a simple variable bench power supply.Actually this is quite important because one of the first projects a hobbyist should undertake is the construction of a variable regulated power supply. While a dedicated

supply is quite handy e.g. 5V or 12V, it's much handier to have a variable supply onhand, especially for testing. Most digital logic circuits and processors need a 5-volt power supply. To use these parts we need to build a regulated 5-volt source. Usually you start with an unregulated power supply ranging from 9 volts to 24 volts DC (A 12 volt power supply is included with the [Beginner Kit](http://www.iguanalabs.com/1stled.htm) and the [Microcontroller Beginner Kit](http://www.iguanalabs.com/mbkit.htm).). To make a 5 volt power supply, we use a LM7805 voltage regulator IC (Integrated Circuit). The IC is shown below.

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The LM7805 is simple to use. You simply connect the positive lead of your unregulated. DC power supply (anything from 9VDC to 24VDC) to the Input pin, connect the negative lead to the Common pin and then when you turn on the power, you get a 5 volt supply from the Output pin.

**2.6.1 Circuit Features:**

**Brief description of operation:** Gives out well regulated +5V output, output current

capability of 100 mA

**Circuit protection:** Built-in overheating protection shuts down output when regulator IC gets too hot

**Circuit complexity:** Very simple and easy to build

**Circuit performance:** Very stable +5V output voltage, reliable operation

**Availability of components:** Easy to get, uses only very common basic components

**Design testing:** Based on datasheet example circuit, I have used this circuit successfully as part of many electronics projects

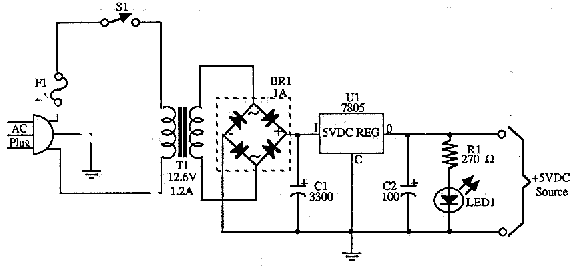
**Applications:** Part of electronics devices, small laboratory power supply

**Power supply voltage:** Unregulated DC 8-18V power supply

**Power supply current:** Needed output current + 5 mA

**Component costs:** Few dollars for the electronics components + the input transformer

**CIRCUIT DIAGRAM:**

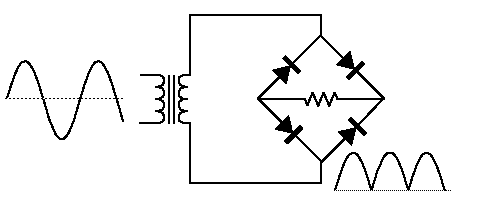
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**Fig : Power Supply Circuit Diagram**

This 5V dc acts as Vcc to the microcontroller. The excess voltage is dissipated as heat via an Aluminum heat sink attached to the voltage regulator.

**Bridge Rectifier:**

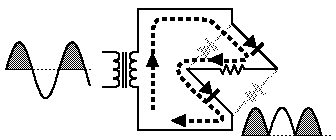
A diode bridge is an arrangement of four diodes connected in a bridge circuit as shown below, that provides the same polarity of output voltage for any polarity of the input voltage. When used in its most common application, for conversion of alternating current (AC) input into direct current (DC) output, it is known as a bridge rectifier. The diagram describes a diode-bridge design known as a full-wave rectifier. This design can be used to rectify single phase AC when no transformer center tap is available. A bridge rectifier makes use of four diodes in a bridge arrangement to achieve full-wave rectification. This is a widely used configuration, both with individual diodes wired as shown and with single component bridges where the diode bridge is wired internally.

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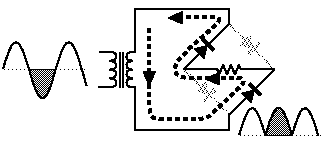
**Typical Bridge Rectifier**

For both positive and negative swings of the transformer, there is a Forward path through the diode bridge. Both conduction paths cause Current to flow in the same direction through the load resistor, accomplishing full-wave rectification. While one set of diodes is forward biased, the other set is reverse biased and effectively eliminated from the circuit.

**Current Flow in the Bridge Rectifier**

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**Current in Bridge Rectifier for + ve half cycle**

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**Current in Bridge Rectifier for -ve half cycle**

**2.7 LM7805 Voltage Regulator:**

**2.7.1 Features:**

• Output Current up to 1A

• Thermal Overload Protection

• Short Circuit Protection

• Output Transistor Safe Operating Area Protection

**2.7.2 Description:**

The MC7805 three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

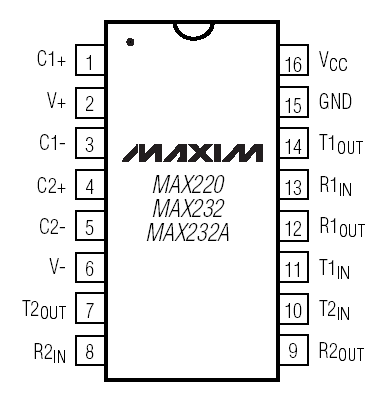
**CHAPTER 3**

**MAX 232**

**3.1 INTRODUCTION:**

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments Lin ASIC™ library.

**PIN DESCRIPTION:**



**3.2 Features:**

* Meet or Exceed TIA/EIA-232-F and ITU Recommended V.28
  + Operates From a Single 5-V Power Supply With 1.0-µF Charge-Pump Capacitors
  + Operate Up To 120 kbit/s
* Two Drivers and Two Receivers
  + ±30-V Input Levels
  + Low Supply Current ...8 mA Typical
  + ESD Protection Exceeds JESD 22
    - 2000-V Human-Body Model (A114-A)
* Upgrade With Improved ESD (15-kV HBM) and 0.1-µF Charge-Pump Capacitors is Available With the MAX202

**3.3 Applications:**

* TIA/EIA-232-F
* Battery-Powered Systems,
* Terminals
* Modems
* Computers

**CHAPTER 4**

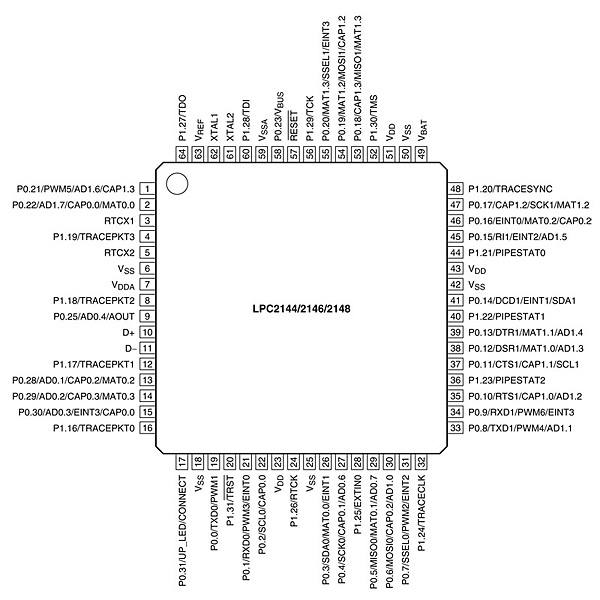
**ARM CONTROLLER**

**4.1 General Description:**

The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine microcontroller with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, LPC2141/42/44/46/48 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit. ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems.

**4.2 Pin Diagram:**

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**4.3 Features:**

* 16-bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.
* 8 kB to 40 kB of on-chip static RAM and 32 kB to 512 kB of on-chip flash
* memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.

* In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot
* loader software. Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1 ms.
* Embedded ICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip Real Monitor software and high-speed tracing of instruction execution.
* USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM. In addition, the LPC2146/48 provides 8 kB of on-chip RAM accessible to USB by DMA.
* One or two (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of

6/14 analog inputs, with conversion times as low as 2.44 μs per channel.

* Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only).
* Two 32-bit timers/external event counters (with four capture and four compare

channels each), PWM unit (six outputs) and watchdog.

* Low power Real-Time Clock (RTC) with independent power and 32 kHz clock input.

* Multiple serial interfaces including two UARTs (16C550), two Fast I2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
* Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
* Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package,.
* Up to 21 external interrupt pins available.
* 60 MHz maximum CPU clock available from programmable on-chip PLL with Settling time of 100 μs.
* On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.

* Power saving modes include Idle and Power-down.
* Individual enable/disable of peripheral functions as well as peripheral clock

scaling for additional power optimization.

* Processor wake-up from Power-down mode via external interrupt or BOD.
* Single power supply chip with POR and BOD circuits:
* CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V

tolerant I/O pads.

**4.4 Functional Description:**

**4.4.1 Architecture Overview:**

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory

systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.The key idea behind Thumb is that of a super-reduced instruction set.

The ARM7TDMI-S processor has two instruction sets:

**•** The standard 32-bit ARM set.

**•** A 16-bit Thumb set.

The Thumb set’s 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM’s performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30% over Thumb mode.

**4.4.2 On-chip Flash Memory:**

The LPC2141/42/44/46/48 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user’s code on LPC2141/42/44/46/48 is 32 kB, 64 kB, 128 kB, 256 kB and 500 kB respectively.The LPC2141/42/44/46/48 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data-retention.

**4.4.3 On-Chip Static RAM:**

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48

provide 8 kB, 16 kB and 32 kB of static RAM respectively. In case of LPC2146/48 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

**4.4.4 Interrupt Controller:**

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast interrupt request (FIQ) has the highest priority. If more than one request isassigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be

assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the

lowest. Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active

**4.4.5 Interrupt sorces:**

Each peripheral device has one interrupt line connected to the Vectored Interrupt

Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

**4.5 Pin Control Block:**

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be consideredundefined.

The Pin Control Module with its pin select registers defines the functionality of the

microcontroller in a given hardware enviroment. After reset all pins of Port 0 and 1 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their JTAG functionality; if trace is enabled, the Trace pins will asume their trace functionality. The pins associated with the I2C0 and I2C1 interface are open drain.

**4.6 Fast General Purpose Parallel I/O (GPIO):**

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins. LPC2141/42/44/46/48 introduce accelerated GPIO functions over prior LPC2000

Devices:

**•** GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.

**•** Mask registers allow treating sets of port bits as a group, leaving other bits

unchanged.

**•** All GPIO registers are byte addressable.

**•** Entire port value can be written in one instruction

**4.6.1 Features:**

**•** Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.

**•** Direction control of individual bits.

**•** Separate control of output set and clear.

**•** All I/O default to inputs after reset.

**4.7 10-Bit ADC:**

The LPC2141/42 contain one and the LPC2144/46/48 contain two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

**4.7.1 Features:**

**•** 10 bit successive approximation analog to digital converter.

**•** Measurement range of 0 V to VREF (2.0 V ≤ VREF ≤ VDDA).

**•** Each converter capable of performing more than 400,000 10-bit samples per second.

**•** Every analog input has a dedicated result register to reduce interrupt overhead.

**•** Burst conversion mode for single or multiple inputs.

**•** Optional conversion on transition on input pin or timer match signal.

**•** Global Start command for both converters (LPC2142/44/46/48 only).

**4.8 10-Bit DAC:**

The DAC enables the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

**4.8.1 Features:**

**•** 10-bit DAC.

**•** Buffered output.

**•** Power-down mode available

**4.9 USB 2.0 Device Controller:**

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2141/42/44/46/48 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

A DMA controller (available in LPC2146/48 only) can transfer data between an endpoint buffer and the USB RAM.

**4.9.1 Features:**

**•** Fully compliant with USB 2.0 Full-speed specification.

**•** Supports 32 physical (16 logical) endpoints.

**•** Supports control, bulk, interrupt and isochronous endpoints.

**•** Scalable realization of endpoints at run time.

**•** Endpoint maximum packet size selection (up to USB maximum specification) by

software at run time.

**•** RAM message buffer size based on endpoint realization and maximum packet size.

**•** Supports SoftConnect and GoodLink LED indicator. These two functions are sharing one pin.

**•** Supports bus-powered capability with low suspend current.

**•** Supports DMA transfer on all non-control endpoints (LPC2146/48 only).

**•** One duplex DMA channel serves all endpoints (LPC2146/48 only).

**•** Allows dynamic switching between CPU controlled and DMA modes (only in

LPC2146/48).

**•** Double buffer implementation for bulk and isochronous endpoints

**4.10 UARTs:**

The LPC2141/42/44/46/48 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2144/46/48 UART1 also provides a full modem control handshake interface.Compared to previous LPC2000 microcontrollers, UARTs in PC2141/42/44/46/48introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baudrates such as 115200 with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware (UART1 in LPC2144/46/48 only).

**4.10.1 Features:**

**•** 16 byte Receive and Transmit FIFOs.

**•** Register locations conform to ‘550 industry standard.

**•** Receiver FIFO trigger points at 1, 4, 8, and 14 bytes

**•** Built-in fractional baud rate generator covering wide range of baud rates without a

need for external crystals of particular values.

**•** Transmission FIFO control enables implementation of software (XON/XOFF) flow

control on both UARTs.

**•** LPC2144/46/48 UART1 equipped with standard modem interface signals. This

module also provides full support for hardware flow control (auto-CTS/RTS).

**4.11 I2C-Bus Serial I/O Controller:**

The LPC2141/42/44/46/48 each contain two I2C-bus controllers. The I2C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the

chip has to initiate a data transfer or is only addressed. The I2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I2C-bus implemented in LPC2141/42/44/46/48 supports bit rates up to 400 kbit/s (Fast I2C-bus).

**4.11.1 Features:**

**•** Compliant with standard I2C-bus interface.

**•** Easy to configure as master, slave, or master/slave.

**•** Programmable clocks allow versatile rate control.

**•** Bidirectional data transfer between masters and slaves.

**•** Multi-master bus (no central master).

**•** Arbitration between simultaneously transmitting masters without corruption of serial

data on the bus.

**•** Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

**•** Serial clock synchronization can be used as a handshake mechanism to suspend and

resume serial transfer.

**•** The I2C-bus c ostic purposes

**4.12 SSI Serial I/O Controller:**

The LPC2141/42/44/46/48 each contain one SPI controller. The SPI is a full duplex Serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given. Data transfer. During a data transfer the master always sends a byte of data to the slave, And the slave always sends a byte of data to the master.

**4.12.1 Features:**

**•** Compliant with Serial Peripheral Interface (SPI) specification.

**•** Synchronous, Serial, Full Duplex, Communication.

**•** Combined SPI master and slave.

**•** Maximum data bit rate of one eighth of the input clock rate.

**4.13 SSP Serial I/O Controller:**

The LPC2141/42/44/46/48 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

**4.13.1 Features:**

**•** Compatible with Motorola’s SPI, TI’s 4-wire SSI and National Semiconductor’s

Micro wire buses.

**•** Synchronous serial communication.

**•** Master or slave operation.

**•** 8-frame FIFOs for both transmit and receive.

**•** Four bits to 16 bits per frame.

**4.14 General Purpose Timers/External Event Counters:**

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them. The LPC2141/42/44/46/48 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

**4.14.1 Features:**

**•** A 32-bit timer/counter with a programmable 32-bit prescaler.

**•** External event counter or timer operation.

**•** Four 32-bit capture channels per timer/counter that can take a snapshot of the timer

value when an input signal transitions. A capture event may also optionally generate

an interrupt.

**•** Four 32-bit match registers that allow:

Continuous operation with optional interrupt generation on match.

Stop timer on match with optional interrupt generation

Reset timer on match with optional interrupt generation.

**•** Four external outputs per timer/counter corresponding to match registers, with the

following capabilities:

Set LOW on match.

Set HIGH on match.

Toggle on match.

Do nothing on match

**4.15 Watchdog Timer:**

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

**4.15.1 Features:**

**•** Internally resets chip if not periodically reloaded.

**•** Debug mode.

**•** Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

**•** Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.

**•** Flag to indicate watchdog reset.

**•** Programmable 32-bit timer with internal pre-scaler.

**•** Selectable time period from (TPCLK × 256 × 4) to (TPCLK × 232 × 4) in multiples of TPCLK × 4.

**4.16 Real-Time Clocks:**

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

**4.16.1 Features:**

**•** Measures the passage of time to maintain a calendar and clock.

**•** Ultra-low power design to support battery powered systems.

**•** Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.

**•** Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the

external crystal/oscillator input at XTAL1. Programmable reference clock divider

allows fine adjustment of the RTC.

**•** Dedicated power supply pin can be connected to a battery or the main 3.3 V.

**4.17 Pulse Width Modulator:**

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2141/42/44/46/48. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requiresthree non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs. Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

**4.17.1 Features:**

**•** Seven match registers allow up to six single edge controlled or three double edge

controlled PWM outputs, or a mix of both types.

**•** The match registers also allow:

Continuous operation with optional interrupt generation on match.

Stop timer on match with optional interrupt generation.

Reset timer on match with optional interrupt generation.

**•** Supports single edge controlled and/or double edge controlled PWM outputs. Single

edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the

output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.

**•** Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.

**•** Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

**•** Match register updates are synchronized with pulse outputs to prevent generation of

erroneous pulses. Software must ‘release’ new match values before they can become

effective.

**•** May be used as a standard timer if the PWM mode is not enabled.

**•** A 32-bit Timer/Counter with a programmable 32-bit Prescaler

**4.18 System Control:**

**4.18.1 Crystal Oscillator:**

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz.The oscillator output frequency is called fosc and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. fosc and CCLK are the same value unless the PLL is running and connected.

**4.18.2 PLL(Phase Locked Loop):**

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The Input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

**4.18.3 Reset And Wake Up Timer:**

Reset has two sources on the LPC2141/42/44/46/48: the RESET pin and watchdog reset. The RESET pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it Is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of VDD ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

**4.18.4 Brown Out Detector:**

The LPC2141/42/44/46/48 include 2-stage monitoring of the voltage on the VDD pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the VIC. This signal can be enabled for interrupt; if not, software can monitor the signal by reading. Dedicated register.

The second stage of low voltage detection asserts reset to inactivate the

LPC2141/42/44/46/48 when the voltage on the VDD pins falls below 2.6 V. This resetprevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset. Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

**4.18.5 Code Security:**

This feature of the LPC2141/42/44/46/48 allow an application to control whether it can be debugged or protected from observation. If after reset on-chip boot loader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

**4.18.6 External Interrupt Inputs:**

The LPC2141/42/44/46/48 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake-up the processor from Power-down mode. Additionally capture input pins can also be used as external interrupts without the

Option to wake the device up from Power-down mode.

**4.18.7 Memory Mapping Control:**

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

**4.18.8 Power Control:**

The LPC2141/42/44/46/48 supports two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses. In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip Power consumption to nearly zero.Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during active and idle mode.

**4.18.9 VPB(VLSI Peripheral Bus):**

The VPB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The VPB divider serves two purposes. The first is to provide peripherals with the desired PCLK via VPB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the VPB bus may be slowed down to 1⁄2 to 1⁄4 of the processor clock rate. Because the VPB bus must work properly at power-up (and its timing cannot be altered if it does not work since the VPB divider control registers reside on the VPB bus), the default condition at reset is for the VPB bus to run at 1⁄4 of the processor clock rate. The second purpose of the VPB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the VPB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

**4.19 Emulation And Debugging:**

The LPC2141/42/44/46/48 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

**4.19.1 Embedded ICE:**

Standard ARM Embedded ICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an Embedded ICE protocol converter. Embedded ICE protocol converter converts the Remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state.

The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-Score. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the Embedded ICE logic.

**4.19.2 Embedded Trace:**

Since the LPC2141/42/44/46/48 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

**4.19.3 Real Monitor:**

Real Monitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the

DCC, which is present in the Embedded ICE logic. The LPC2141/42/44/46/48 contain a specific configuration of Real Monitor software programmed into the on-chip flash memory.

**CHAPTER 5**

**LCD**

**5.1 Introduction:**

Liquid crystal display is very important device in embedded system. It offers high flexibility to user as he can display the required data on it. But due to lack of proper approach to LCD interfacing many of them fail. Many people consider LCD interfacing a complex job but according to me LCD interfacing is very easy task, you just need to have a logical approach. This page is to help the enthusiast who wants to interface LCD with through understanding. Copy and Paste technique may not work when an embedded system engineer wants to apply LCD interfacing in real world projects.

You will be knowing about the booster rockets on space shuttle. Without these booster rockets the space shuttle would not launch in geosynchronous orbit. Similarly to understand LCD interfacing you need to have booster rockets attached! To get it done right you must have general idea how to approach any given LCD.This page will help you develop logical approach towards LCD interfacing.

First thing to begin with is to know what LCD driver/controller is used in LCD.Yes, your LCD is dumb it does not know to talk with your microcontroller. LCD driver is a link between the microcontroller and LCD. You can refer the datasheet of LCD to know the LCD driver for e.g. JHD 162A is name of LCD having driver HD44780U.You have to interface the LCD according to the driver specification. To understand the algorithm of LCD interfacing user must have datasheet of both LCD and LCD driver. Many people ignore the datasheets and end up in troubles. If you want to interface LCD successfully you must have datasheets.

Why people ignore datasheets? Most of us do not like to read 100 pages of datasheet. But for a accurate technical specification datasheets are must. I will show you a technique to manipulate a datasheet within minutes.

First thing to find out in datasheet is the features viz. operating voltage, type of interface, maximum speed for interface in MHz, size of display data RAM, number of pixels, bits per pixel, number of row and columns. You must have the pin diagram of LCD.Pin diagram of LCD driver can be omitted.

Study the type of communication protocol whether it is parallel or serial interface. Check how LCD discriminates data bytes and command bytes, which pins on LCD are used for communication. Study Interface timing diagram given in the datasheet.

From datasheet of LCD driver find out whether hardware reset is required at startup, what is the time of reset pulse, is it active low and which pins of LCD are to be toggled.

Major task in LCD interfacing is the initialization sequence. In LCD initialization you have to send command bytes to LCD. Here you set the interface mode, display mode, address counter increment direction, set contrast of LCD, horizontal or vertical addressing mode, color format. This sequence is given in respective LCD driver datasheet. Studying the function set of LCD lets you know the definition of command bytes. It varies from one LCD to another. If you are able to initialize the LCD properly 90% of your job is done.

Next step after initialization is to send data bytes to required display data RAM memory location. Firstly set the address location using address set command byte and than send data bytes using the DDRAM write command. To address specific location in display data RAM one must have the knowledge of how the address counter is incremented.

**LCD DISPLAY:**

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**5.2 Features:**

* HIGH CONTRAST LCD SUPERTWIST DISPLAY
* EA DIP162-DNLED: YELLOW/GREEN WITH LED BACKLIGHT
* EA DIP162-DN3LW AND DIP162J-DN3LW WITH WHITE LED B/L., LOPOWER
* INCL. HD 44780 OR COMPATIBLE CONTROLLER
* INTERFACE FOR 4- AND 8-BIT DATA BUS
* POWER SUPPLY +5V OR ±2.7V OR ±3.3V
* OPERATING TEMPERATURE 0~+50°C (-DN3LW, -DHNLED: -20~+70°C)
* LED BACKLIGHT Y/G max. 150mA@+25°C
* LED BACKLIGHT WHITE max. 45mA@+25°C
* SOME MORE MODULES WITH SAME MECHANIC AND SAME PINOUT:
* -DOTMATRIX 1x8, 4x20
* -GRAPHIC 122x32
* NO SCREWS REQUIRED: SOLDER ON IN PCB ONLY
* DETACHABLE VIA 9-PIN SOCKET EA B200-9 (2 PCS. REQUIRED)

**CHAPTER 6**

**6.1 KEIL COMPILER:**

Keil is an IDE(Integrated Development Environment) which is used to develop an application program , compile and run it Even the code can be debugged .It is a simulator where we can check the application code even in the absence of the hardware board.

Keil is also a cross compiler The process of development of the soft code on a processor for a particular application and which can be implemented on the target processor is known as Cross Development.

In our design the main heart of the hardware module is the micro controller which is the programmable IC .The programming language used for developing the software to the micro controller is Embedded C /Assembly. The KEIL cross compiler is used to edit ,compile and debug this program Micro Flash programmer is used for burning the developed code on Keil in to the micro controller Chip.

**6.2 PROGRAM:**

#include<LPC214X.h>

#include<stdio.h>

#include<string.h>

#include"LPCCOM.h"

#include"LPCLCD.h"

int x=0;

int main()

{

VPBDIV=1;

Seril\_Init(0,9600,9600);

Com0\_Int\_Enable();

lcd\_init();//message(0x80,"COM to LCD");//Trans\_Str(0,"ENTER DATA");

delay(10000);

memset(S\_Buf,'0',32);

command\_data(0x01,0);

while(1)

{

command\_data(0x80,0);

for(x=0;x<16;x++)

{

command\_data(S\_Buf[x],1);

if(S\_Buf[x]=='%')

{

command\_data(0x01,0);

memset(S\_Buf,'0',32);

}

if(S\_Buf[x]==13)

{

while(1)

{

command\_data(0x18,0);

delay(2000);

}

}

}

command\_data(0xC0,0);

for(x=0;x<16;x++)

{

command\_data(S\_Buf[x+16],1);

if(S\_Buf[x+16]=='%')

{

command\_data(0x01,0);

memset(S\_Buf,'0',32);

}

if(S\_Buf[x+16]==13)

{

while(1)

{

command\_data(0x18,0);

delay(2000);

}

}

}

}

}

**APPLICATIONS:**

* Organizational Applications
* Monitoring sections in Research centres
* Transportation Applications,
* Such as indication of rule on national highways.
* And also one of the most important requirements
* for the message Information in Railway Stations,
* Bus Stations etc.,

**ADVANTAGES:**

* Due to their tiny size and low power consumption, LPC2148 are ideal for applications where miniaturization is a key requirement, such as access control
* The relative simplicity of ARM processors made them suitable for low power applications
* Cost effective and more efficiency due to LED display and ARM processor

**CONCLUSION:**

* The main objective of the project is to interface an LCD with microcontroller and display the moving message on to the LCD. The software used to program is a keil compiler
* Very good advertising results are obtained from these unique displays with latest technology. You can change the message as often as you want with ordinary computer keyboard without any prior experience of any kind LCDs available
* Moving message on LCD are ideal for all type of commercial establishments like Hotels, Restaurants, Retail Shops, Banks, Airports, Clinics, Hospitals and other such places to get maximum attention of people.
* This scrolling message board is not a simple message box. Instead of showing a static text, it scrolls the text to maximize visitors attention.
* Have the scope to display scrolling messages through mobile internet devices

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